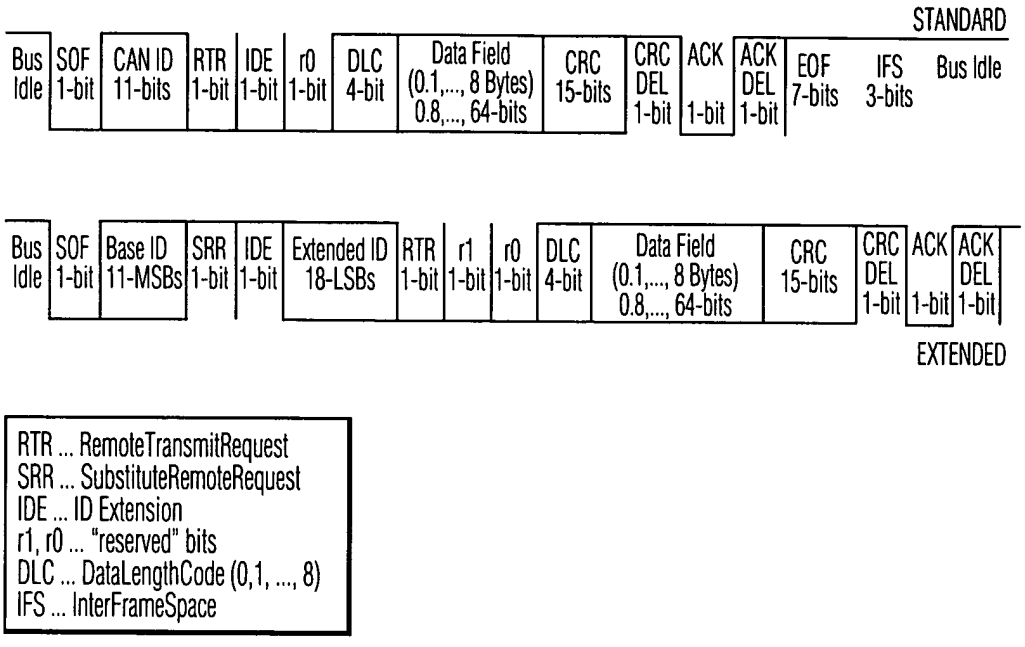
STANDARD
Bus Idle
SOF 1-bit
CAN ID 11-bits
RTR 1-bit
IDE 1-bit
r0 1-bit
DLC 4-bit
Data Field (0.1,..., 8 Bytes) 0.8,..., 64-bits
CRC 15-bits
CRC DEL 1-bit
ACK 1-bit
ACK DEL 1-bit
EOF 7-bits
IFS 3-bits
Bus Idle
Bus Idle
SOF 1-bit
Base ID 11-MSBs
SRR 1-bit
IDE 1-bit
Extended ID 18-LSBs
RTR 1-bit
r1 1-bit
r0 1-bit
DLC 4-bit
Data Field (0.1,..., 8 Bytes) 0.8,..., 64-bits
CRC 15-bits
CRC DEL 1-bit
ACK 1-bit
ACK DEL 1-bit
EXTENDED
RTR ... RemoteTransmitRequest
SRR ... SubstituteRemoteRequest
IDE ... ID Extension
r1, r0 ... "reserved" bits
DLC ... DataLengthCode (0,1, ..., 8)
IFS ... InterFrameSpace

FIG. 1

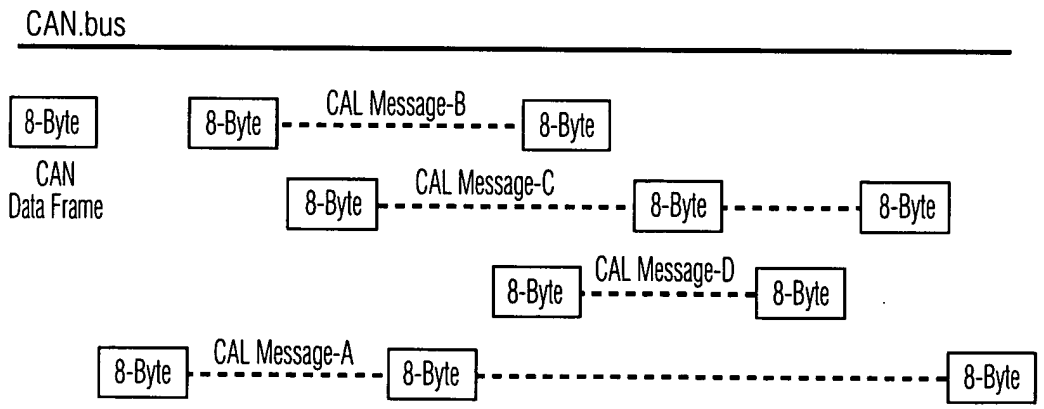
CAN.bus
8-Byte
CAN Data Frame
8-Byte
CAL Message-B
8-Byte
8-Byte
CAL Message-C
8-Byte
8-Byte
8-Byte
CAL Message-D
8-Byte
8-Byte
8-Byte
CAL Message-A
8-Byte
8-Byte

FIG. 2

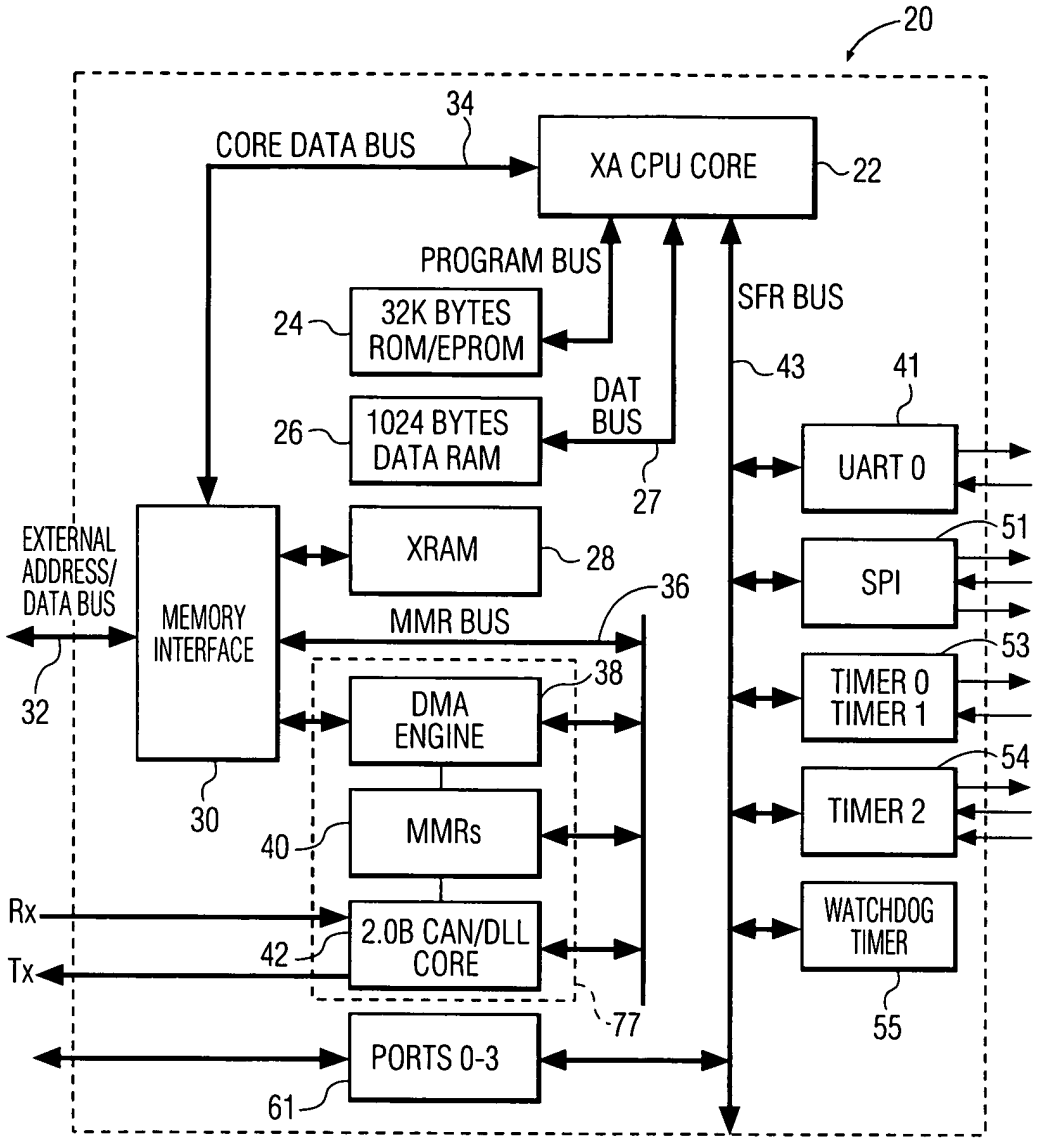
20
34
CORE DATA BUS
XA CPU CORE
22
PROGRAM BUS
SFR BUS
24
32K BYTES ROM/EPROM
43
41
DAT BUS
26
1024 BYTES DATA RAM
27
UART 0
EXTERNAL ADDRESS/ DATA BUS
MEMORY INTERFACE
XRAM
28
51
SPI
36
MMR BUS
53
TIMER 0 TIMER 1
32
38
DMA ENGINE
54
TIMER 2
30
40
MMRs
Rx
2.0B CAN/DLL CORE
WATCHDOG TIMER
42
Tx
77
55
PORTS 0-3
61

FIG. 3

MMRs

MMR name	R/W?	Reset	Access	Address Offset	Description
Message Object Registers (n = 0 - 31)					
MnMIDH	R/W	x....x00b	Word only	000$n_4n_3n_2n_1n_0$0000b (n0h)	Message n Match ID High
MnMIDL	R/W	xxxxh	Word only	000$n_4n_3n_2n_1n_0$0010b (n2h)	Message n Match ID Low
MnMSKH	R/W	x....x000b	Word only	000$n_4n_3n_2n_1n_0$0100b (n4h)	Message n Mask High
MnMSKL	R/W	xxxxh	Word only	000$n_4n_3n_2n_1n_0$0110b (n6h)	Message n Mask Low
MnCTL	R/W	00000xxxb	Byte/Word	000$n_4n_3n_2n_1n_0$1000b (n8h)	Message n Control
MnBLR	R/W	xxxxh	Word only	000$n_4n_3n_2n_1n_0$1010b (nAh)	Message n Buffer Location
MnBSZ	R/W	00000xxxb	Byte/Word	000$n_4n_3n_2n_1n_0$1100b (nCh)	Message n Buffer Size
MnFCR	R/W	00xxxxxxb	Byte/Word	000$n_4n_3n_2n_1n_0$1110b (nEh)	Message n Fragmentation Count
CIC Registers					
MCPLL	R/C	0000h	Byte/Word	224h	Message Complete Low
MCPLH	R/C	0000h	Byte/Word	226h	Message Complete High
CANINTFLG	R/C	0000h	Byte/Word	228h	CAN Interrupt Flag Register
MCIR	RO	0000h	Byte/Word	229h	Message Complete Info Reg.
MEIR	RO	0000h	Byte/Word	22Ah	Message Error Info Register
FESTR	R/C	0000h	Byte/Word	22Ch	Frame Error Status Register
FEENR	R/W	0000h	Byte/Word	22Eh	Frame Error Enable Register
SCP/SPI Registers					
SPICFG	R/W	0000h	Byte/Word	260h	SCP/SPI Configuration
SPIDATA	R/W	00h	Byte/Word	262h	SCP/SPI Data
SPICS	R/W	00h	Byte/Word	263h	SCP/SPI Control and Status
CCB Registers					
CANCMR	R/W	01h	Byte/Word	270h	CAN Command Register
CANSTR	R/O	00h	Byte/Word	271h	CAN Status Register
CANBTR	R/W	00h	Byte/Word	272h	CAN Bus Timing Reg. (low)
-	R/W	00h	Byte/Word	273h	CAN Bus Timing Reg. (high)
TXERC	R/W*	00h	Byte/Word	274h	Tx Error Counter
RXERC	R/W*	00h	Byte/Word	275h	Rx Error Counter
EWLR	R/W	96h	Byte/Word	276h	Error Warning Limit Register
ECCR	RO	0000h	Byte/Word	278h	Error Code Capture Register
ALCR	RO	0000h	Byte/Word	27Ah	Arbitration Lost Capture Reg.
RTXDTM	WO	0000h	Byte/Word	27Ch	RTX Data Test Mode
GCTL	R/W	0000h	Byte/Word	27Eh	Global Control Byte
MIF Registers					
XRAMB	R/W	FEh	Byte/Word	290h	XRAM Base Address
MBXSR	R/W	FFh	Byte/Word	291h	Msg. Buff./XRAM Seg. Reg.
MIFBTRL	R/W	EFh	Byte/Word	292h	MIF Bus Timing Reg. Low
MIFBTRH	R/W	FFh	Byte/Word	293h	MIF Bus Timing Reg. High

Legend: R/W = Read & Write, RO = Read Only, WO = Write Only, R/C = Read & Clear, W* = Writable only during CAN Reset mode, x = undefined after reset.

FIG. 4

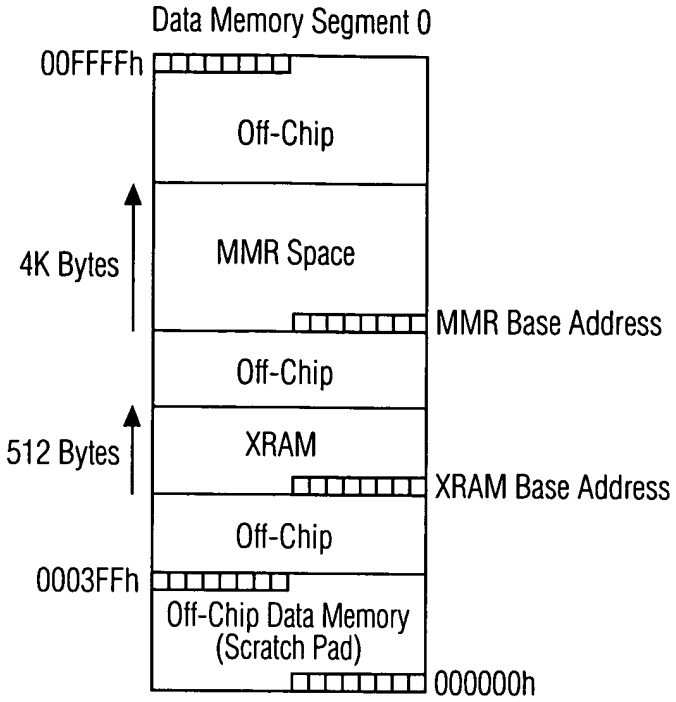
Data Memory Segment 0
00FFFFh
Off-Chip
4K Bytes
MMR Space
MMR Base Address
Off-Chip
512 Bytes
XRAM
XRAM Base Address
Off-Chip
0003FFh
Off-Chip Data Memory
(Scratch Pad)
000000h

FIG. 5

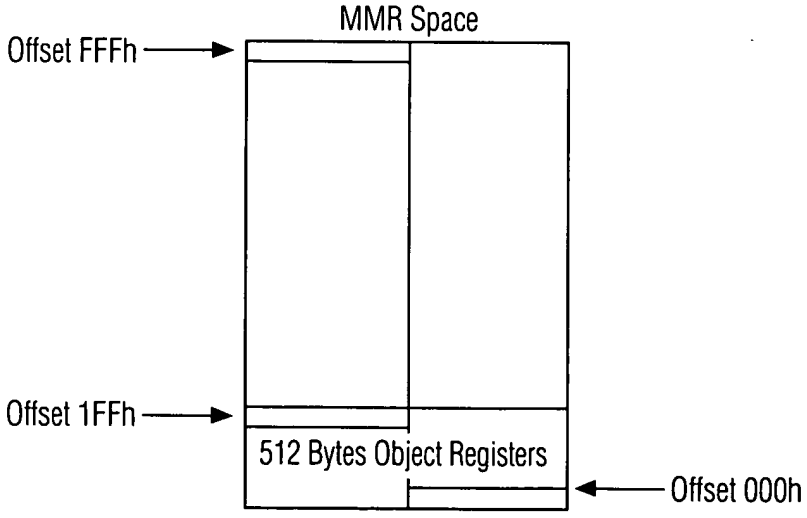
MMR Space
Offset FFFh
Offset 1FFh
512 Bytes Object Registers
Offset 000h

FIG. 6

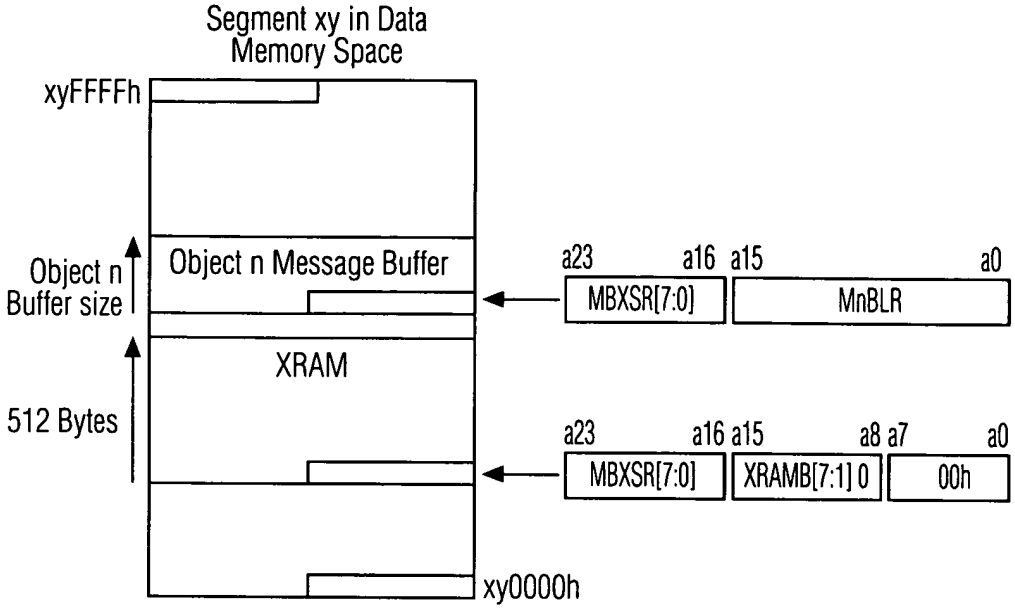
Segment xy in Data
Memory Space
xyFFFFh
Object n
Buffer size
Object n Message Buffer
XRAM
512 Bytes
xy0000h
a23
a16
a15
a0
MBXSR[7:0]
MnBLR
a23
a16
a15
a8
a7
a0
MBXSR[7:0]
XRAMB[7:1] 0
00h

FIG. 7

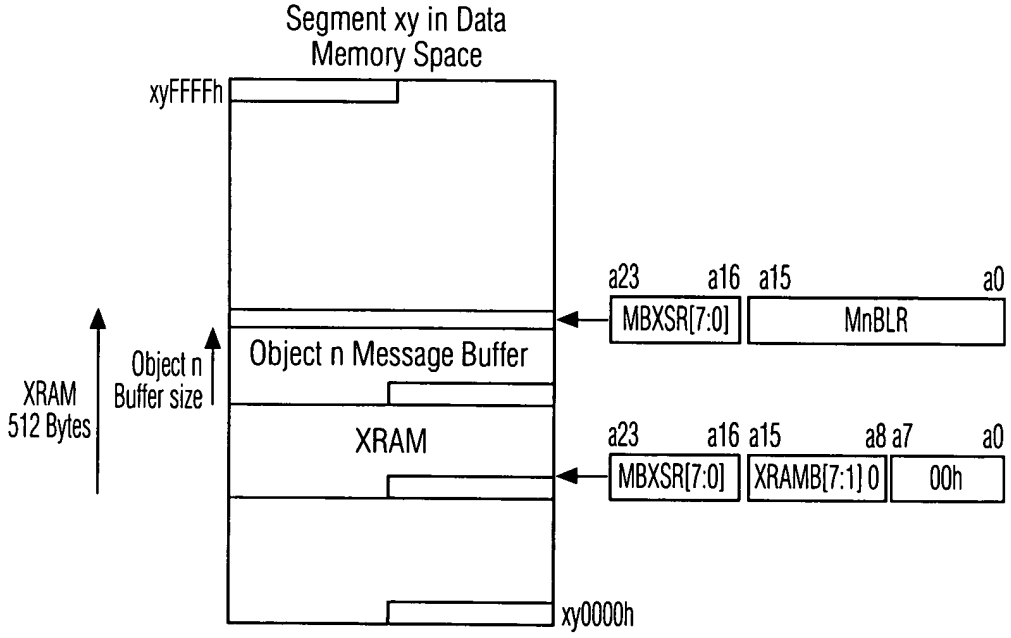
Segment xy in Data
Memory Space
xyFFFFh
XRAM
512 Bytes
Object n
Buffer size
Object n Message Buffer
XRAM
xy0000h
a23
a16
a15
a0
MBXSR[7:0]
MnBLR
a23
a16
a15
a8
a7
a0
MBXSR[7:0]
XRAMB[7:1] 0
00h

FIG. 8

Object n Match ID Field (MnMIDH and MnMIDL)

Mid28 – Mid18	Mid17 – Mid10	Mid9 – Mid2	Mid1	Mid0	MIDE

Object n Mask Field (MnMSKH and MnMSKL)

Msk28 – Msk18	Msk17 – Msk10	Msk9 – Msk2	Msk1	Msk0

Screener ID Field (assembled from incoming bit-stream)

CAN ID.28 – CAN ID.18	Data Byte 1 [7:0]	Data Byte 2 [7:0]	x	x	IDE

FIG. 9

Object n Match ID Field (MnMIDH and MnMIDL)

Mid28 – Mid18	Mid17 – Mid10	Mid9 – Mid2	Mid1	Mid0	MIDE

Object n Mask Field (MnMSKH and MnMSKL)

Msk28 – Msk18	Msk17 – Msk10	Msk9 – Msk2	Msk1	Msk0

Screener ID Field (assembled from incoming bit-stream)

CAN ID.28 – CAN ID.0	IDE

FIG. 10

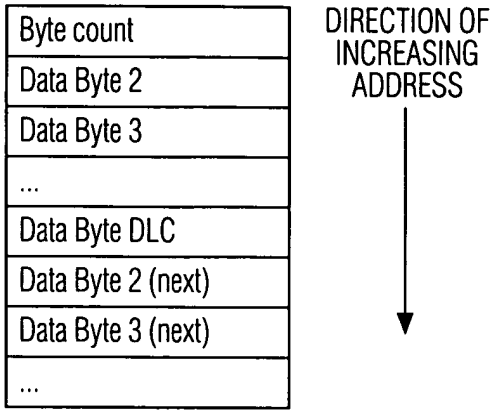
Byte count
Data Byte 2
Data Byte 3
...
Data Byte DLC
Data Byte 2 (next)
Data Byte 3 (next)
...
DIRECTION OF INCREASING ADDRESS

FIG. 11

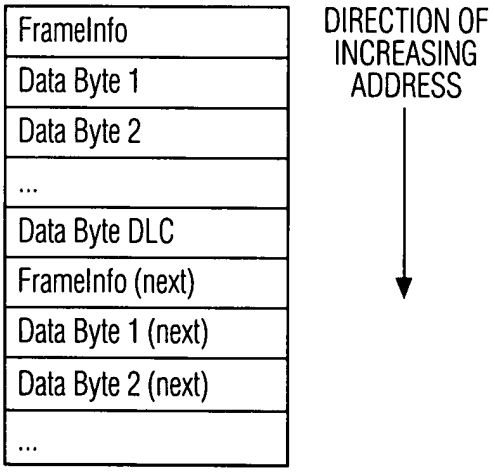
FrameInfo
Data Byte 1
Data Byte 2
...
Data Byte DLC
FrameInfo (next)
Data Byte 1 (next)
Data Byte 2 (next)
...
DIRECTION OF INCREASING ADDRESS

FIG. 12